

REMARKS

The Examiner's indication of allowability of claims 3-8, if rewritten in independent form, is acknowledged and appreciated.

Claim 11 has been amended as required.

Claims 1-24 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Aji et al. Applicant's respectfully traverse this rejection because the cited reference does not disclose (or suggest) the feature of the present invention for constructing a gadget graph from a tile graph such that feasible buffered routings of every net are in one-to-one correspondence to simple paths between a net source and a net sink in the gadget graph, as described in independent claims 1 and 23.

The Aji et al. reference relates to an algorithm for performing constraints-based global routing step in the physical design of integrated circuits. The algorithm of Aji et al. works by (1) finding a set of at least one feasible route for each net; (2) constructing an intersection graph in which every node represents a net, and an edge between nodes *u* and *v* indicates that the respective feasible routes intersect at least one point of the routing grid (with the edge weights capturing the degree of incompatibility between feasible routings corresponding to end nodes); and (3) partitioning the intersection graph and selecting feasible routes for nets in each partition using integer programming methods. Since nodes of the intersection graph of Aji et al. represent nets and not points on the routing grid (see Fig. 9 of Aji et al.), paths in the intersection graph cannot be placed in one-to-one correspondence to the feasible buffered routings, as in the gadget graph of the present invention. For this

reason, claims 1 and 23 and their respective dependent claims 2-22 and 24 are allowable over Aji et al.

For all of the above reasons, Applicants request reconsideration and allowance of the claimed invention. The Examiner should contact Applicants' undersigned attorney if a telephone conference would expedite prosecution.

Respectfully submitted,

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